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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,400	04/12/2004	German R. Gutierrez	BU1647C2	2892

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EXAMINER	
TSE, YOUNG TOI	
ART UNIT	PAPER NUMBER
2611	
MAIL DATE	DELIVERY MODE
06/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/822,400	GUTIERREZ ET AL.	
	Examiner	Art Unit	
	YOUNG T. TSE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on February 29, 2008 have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argues that the split loop filter 63 of Volk is coupled to the charge pump 62, and not to a detector, as recited in claim 1. The examiner respectfully disagrees, as shown in Figure 3 of Volk's PLL circuit, although the split filter 63 is not directly connected to the phase detection/comparison circuit 61, clearly, the split filter 63 is coupled to the phase detection/comparison circuit 61 for filtering the detector output signal through the charge pump 62, as recited in claim 1 (emphasis added). Applicant further argues that the second integrator 450 of Everitt does not disclose a "second filter," as recited in claim 1. The examiner disagrees, although Everitt does not explicitly show, suggest or teach the second integrator 450 is a "second filter, it is well known to a skilled person in the art to know that a filter can be performed or integrated as an integrator. For example, the newly cited reference, Fukahori et al. (U.S. Patent No. 4,374,335) discloses a PLL circuit in Figure 2 which comprises a phase detector/comparator 26, a filter 22, and an Oscillator 24. The filter 22 is integrated by integrator circuits and current sources to provide filter signals to the Oscillator 24 which is similar to the second integrator 450 shown in Everitt's PLL circuit 400.

Regarding claim 3, Applicant argues that the digital divider 67 shown in Volk's PLL circuit 60 is not a frequency divider. The examiner respectfully disagrees, clearly, Volk teaches that "the current I_{OS2} is output from the variable gain current source 65 is then applied to VCO 66 to generate the Θ_{FB} feedback signal via digital divider 67. The frequency of the Θ_{FB} signal generated by VCO 66 is directly proportional to the amount of the I_{OS2} current such that PLL 60 is brought back to the locked condition." See Col. 9, lines 4-9. It is also well known to a skilled person in the art to know that a divider coupled between an Oscillator and a phase detector of a PLL circuit is a frequency divider, including the divider 124 shown in the prior art Figure 1 of the instant application.

Therefore, the independent claim 1, including the dependent claims 2-5 and 8 are unpatentable over Volk in view Everitt, and further in view of Voorman and/or Hotine.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Volk (U.S. Patent No. 5,384,502) in view of Everitt et al. (U.S. Patent No. 6,188,739, hereinafter "Everitt").

Regarding claim 1, Volk discloses a phase locked loop (PLL) circuit 60 in Figure 3 comprising a phase comparison circuit 61 which receives an external data input signal Θ_D and a reference signal Θ_{FB} to generate a phase detected output signal (PD and/or UP) indicative of a difference between the input signal and the reference signal; a split loop filter 63 which filters the phase detected output signal through a charge pump 62 to provide a filtered output signal; a trans-conductance (gm) amplifier 64 which amplifies the filtered output signal to generate a current output signal I_{OS}; a variable gain current source 65 which receives the current output signal I_{OS} and a first current output signal I_{OS1} to generate a second current output signal I_{OS2}; a VCO 66 which receives the second current output signal I_{OS2} to generate an oscillator signal; and a frequency divider 67 which divides the frequency of the oscillator signal to generate the reference signal. Although Volk does not show or suggest that a second filter is used coupled between the trans-conductance (gm) amplifier 64 and the VCO 66 to further filter the

current output signal I_{OS} from the trans-conductance (gm) amplifier 64 before controlling the oscillator signal of the VCO 66.

Everitt also discloses a PLL circuit 400 in Figure 4 comprising similar circuitries of Volk's PLL circuit. Further, the PLL circuit also includes a second integrator (second filter) 450 coupled between a charge pump (sometime also called trans-conductance (gm) amplifier) and a signal controlled oscillator (VCO) 416 to generate a current signal to the VCO 416 in order to generate a reference signal to the phase or frequency comparator circuit 404. Also see Col. 4, line 39 to Col. 5, line 18.

Therefore, it would have been obvious to one of ordinary skill in the art to add an additional filter prior Volk's VCO 66 of the PLL circuit 60 as taught by Everitt for the purpose of further or additionally filtering, for example, the current signal of the trans-conductance (gm) amplifier 64 prior controlling the frequency by the VCO 66.

Regarding claim 2, the split loop filter 63 shown in Figure 4 is indicated as a single-pole RC filter.

Regarding claim 3, the frequency divider 67 is coupled to the VCO 66 and divided the oscillator signal to generate the reference signal to the phase comparison circuit 61.

Regarding claim 4, the external data input signal Θ_D is a serial data stream.

Regarding claim 5, it is well known to a person skill in the art to know that the serial data stream of the external data input signal Θ_D could be operated at a data rate of at least 2.488 Ghz if Volk's PLL circuit 60 is used in a SONET OC-48 transceiver as

pointed out at least in the Background of the Invention of the instant application on page 3, lines 8-12.

Regarding claim 8, the reference signal used in the phase comparison circuit 61 is a reference clock signal generated by the VCO 66 through the frequency divider 67.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Volk in view of Everitt as applied to claim 1 above, and further in view of Voorman (U.S. Patent No. 4,780,690).

Regarding claim 6, although Volk discloses that the trans-conductance (gm) amplifier 64 shown in Figure 4 comprises amplifiers receiving the filtered signal of the split loop filter 63 and a current load circuit coupled to the amplifiers to provide the current signal $I_{OS,}$ Volk fails to teach or suggest that the amplifiers are differential amplifiers.

Voorman relates to a filter arrangement having a trans-conductance circuit shown in Figure 1, wherein the trans-conductance circuit, for example, shown in Figure 3 comprises two differential amplifiers receiving the filtered signal of the filter arrangement of Figure 1 and a current load circuit I_5 coupled to the differential amplifiers to provide a current signal. Also see Col. 5, lines 1-24.

Therefore, it would have been obvious to one of ordinary skill in the art that Volk's trans-conductance (gm) amplifier 64 of the PLL circuit 60 is capable of or being integrated by a differential amplifier and a current load circuit as taught by Voorman in order to generate a current signal from a current of a filter.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Volk in view of Everitt as applied to claim 1 above, and further in view of Hotine (U.S. Patent No. 4,656,647).

Regarding claim 7, although Volk does not show or suggest that the output signal of the phase comparison circuit 61 of the PLL circuit 60 has a peak to peak signal swing of less than one volt.

Hotine discloses a PLL circuit in Figure 2 comprising a phase comparator 45, a low pass filter 48 and a VCO 50, wherein the phase comparator 45 compares a voltage output signal 42 having a 0.2 peak to peak voltage through a squaring amplifier 43 with an oscillator voltage generated from the VCO 50. Obviously, the voltage at the output signal 47 of the phase comparator 45 has a peak to peak signal of less than one volt. Also see Col. 8, line 45 to Col. 9, line 25.

Therefore, it would have been obvious to one of ordinary skill in the art as taught by Hotine that Volk's phase comparison circuit 61 of the PLL circuit 60 is capable of generating a voltage swing, for example, has a peak to peak signal of less than one volt in order to reduce the voltage of a voltage supply of the PLL circuit 60.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fukahori et al. relates to a PLL circuit comprises a phase detector/comparator, a, oscillator, and a filter, wherein the filter is integrated by integrators and current sources.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is 571- 272-3051. The examiner can normally be reached on Monday-Friday 10:00-6:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on 571- 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/YOUNG T. TSE/
Primary Examiner, Art Unit 2611